

316340

25226

3 Hours / 70 Marks

Seat No. 

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- Instructions* – (1) All Questions are *Compulsory*.  
(2) Answer each next main Question on a new page.  
(3) Illustrate your answers with neat sketches wherever necessary.  
(4) Figures to the right indicate full marks.  
(5) Assume suitable data, if necessary.  
(6) Mobile Phone, Pager and any other Electronic Communication devices are not permissible in Examination Hall.

**Marks**

1.      **Attempt any FIVE of the following :** **10**
- a) Define:
    - i)    Metastability
    - ii)   Fan-Out.
  - b) List any two features of CPLD and FPGA.
  - c) Define the VHDL data types:
    - i)    Scalar
    - ii)   Composite.
  - d) List any two logical operators used in VHDL programming.
  - e) Define VHDL and list different styles of modelling.
  - f) List sequential statements in VHDL programming.
  - g) Differentiate between concurrent and sequential statements in VHDL. (any two)

P.T.O.

- 2. Attempt any THREE of the following : 12**
- a) Describe the working of a MOS transistor as a switch.
  - b) Draw ASIC design flow. Explain any one block.
  - c) State the syntax of a signal and a variable in VHDL programming with one example.
  - d) Write a VHDL program for a half adder using structural modeling.
- 3. Attempt any THREE of the following : 12**
- a) Draw and explain the block diagram of a Moore machine.
  - b) Sketch the CMOS logic circuits for a 2-input AND gate and explain its operation.
  - c) Explain various data types used in VHDL.
  - d) Implement a 4-bit up/down counter using VHDL code.
- 4. Attempt any THREE of the following : 12**
- a) Design a logic circuit for  $Z=AB+CD$  using CMOS NAND gates.
  - b) Draw and explain the architecture of CPLD.
  - c) Compare VHDL and Verilog based on their synthesis capabilities and data types.
  - d) Write a VHDL program using concurrent statements for a 4:1 multiplexer.
  - e) Describe simulators: event-based and cycle-based.

- 5. Attempt any TWO of the following : 12**
- a) Explain the complete CMOS fabrication process using the p-well method with a neat cross-sectional diagram at each major step.
  - b) Write a VHDL program to implement a 3:8 decoder.
  - c) Describe the Boolean optimization processes used in HDL synthesis: flattening, factoring, and mapping.
- 6. Attempt any TWO of the following : 12**
- a) Describe the purpose of the essential elements: Library Declaration, Entity, and Architecture with examples in the VHDL program.
  - b) Develop a VHDL test bench code for a full adder circuit.
  - c) List any four components of the HDL design flow process and explain.
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